

This listing of claims will replace all prior versions and listings of claims in the application.

**Listing of Claims**

- 1.-27. (Cancelled)
28. (Previously presented) A method of forming a semiconductor structure, the method comprising:  
providing a strained semiconductor layer;  
providing a SiGe layer over said strained semiconductor layer; and  
selectively removing said SiGe layer to expose said strained semiconductor layer.
29. (Previously presented) The method of claim 28, wherein said strained semiconductor layer comprises Si, Ge, or GaAs.
30. (Previously presented) The method of claim 28, further comprising, before the step of providing a strained semiconductor layer, providing a relaxed semiconductor layer beneath said strained semiconductor layer.
31. (Previously presented) The method of claim 30, wherein said relaxed semiconductor layer comprises Si or Ge.
32. (Previously presented) The method of claim 28, wherein said strained semiconductor layer is disposed over a semiconductor substrate.
33. (Previously presented) The method of claim 32, wherein said semiconductor substrate comprises Si.
34. (Previously presented) The method of claim 32 wherein said semiconductor substrate comprises an insulator layer.
35. (Previously presented) The method of claim 34, wherein said insulator layer comprises silicon dioxide.
36. (Previously presented) The method of claim 28, wherein said step of selectively removing said SiGe layer comprises thermal oxidation.
37. (Previously presented) The method of claim 36, wherein said thermal oxidation is performed at or below a temperature of approximately 850°C.

38. (Previously presented) The method of claim 36, wherein said thermal oxidation is performed at a temperature at or below approximately 700°C.
39. (Previously presented) The method of claim 28, wherein said step of selectively removing said SiGe layer comprises chemical oxidation.
40. (Previously presented) The method of claim 28, wherein said step of selectively removing said SiGe layer is performed on a first region of said SiGe layer and not on a second region of said SiGe layer.
41. (Previously presented) The method of claim 40, wherein said method further comprises forming a MOSFET in said first region.
42. (Previously presented) The method of claim 41, wherein said MOSFET comprises a high-k dielectric.
43. (Previously presented) The method of claim 40, wherein said method further comprises forming a MOSFET in said second region.
44. (Previously presented) The method of claim 43, wherein said MOSFET comprises a high-k dielectric.
45. (Currently amended) The method of claim 40, wherein said method further comprises:  
forming a surface channel device having a first channel in said first region; and  
forming a buried channel device having a second channel in said second region,  
wherein the strained semiconductor layer comprises said first channel and said second channel.
46. (Previously presented) A method of manufacturing a semiconductor device, comprising:  
providing a strained semiconductor layer;  
providing a SiGe layer over said strained semiconductor layer;  
selectively removing said SiGe layer to expose said strained semiconductor layer;  
providing a gate dielectric over said strained semiconductor layer;  
providing a source region in a first region of said strained semiconductor layer;  
providing a drain region in a second region of said strained semiconductor layer; and  
providing a gate contact disposed above said gate dielectric and between said source and drain regions.

47. (Previously presented) The method of claim 46, wherein said source region and said drain region are p-type doped.
48. (Previously presented) The structure of claim 46, wherein said source region and said drain region are n-type doped.
49. (Previously presented) The method of claim 46, wherein said strained semiconductor layer comprises Si, Ge, or GaAs.
50. (Previously presented) The method of claim 46, further comprising, before the step of providing a strained semiconductor layer, providing a relaxed semiconductor layer beneath said strained semiconductor layer.
51. (Previously presented) The method of claim 50, wherein said relaxed semiconductor layer comprises Si or Ge.
52. (Previously presented) The method of claim 46, wherein said strained semiconductor layer is disposed over a semiconductor substrate.
53. (Previously presented) The method of claim 52, wherein said semiconductor substrate comprises Si.
54. (Previously presented) The method of claim 52 wherein said semiconductor substrate comprises an insulator layer.
55. (Previously presented) The method of claim 52 wherein said gate dielectric comprises a high-k dielectric.